Frequency Synchronization in FPGA

Contents

Need for frequency synchronization

- Frequency synchronization is two clock signals pulse at the same frequency.
- Carrier networks have a strong requirement of frequency synchronization across the network. for example SONET/SDH,OTN,SyncE ...

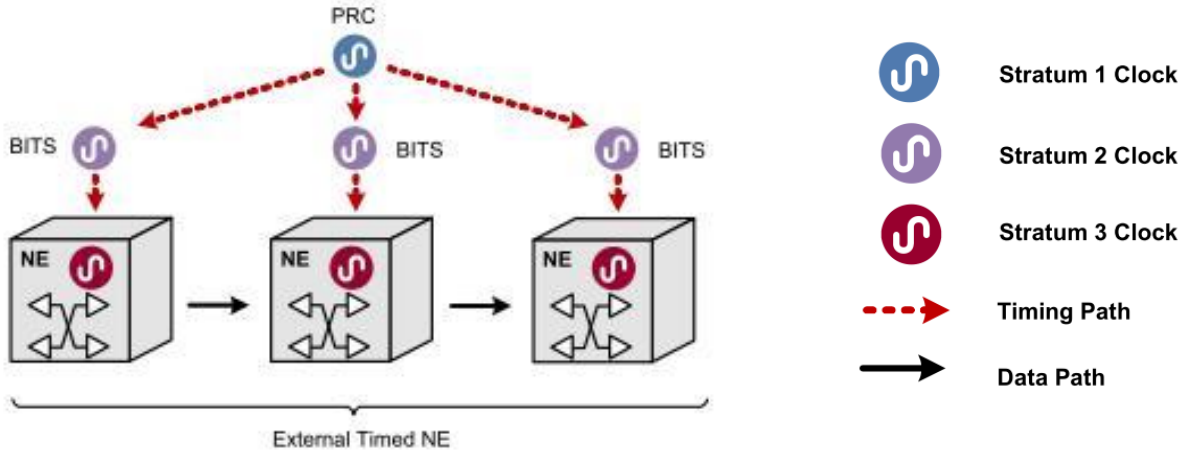
Synchronization of SONET/SDH

- SONET/SDH Networks require precise frequency synchronization at each of its data interfaces for efficient transfer of information.
- Each SONET/SDH Network Element(NE) can be provisioned to free run from an internal oscillator, line timed from an incoming optical interface, or get external timing from the digital synchronization network via external references.

External Timing and Line Timing

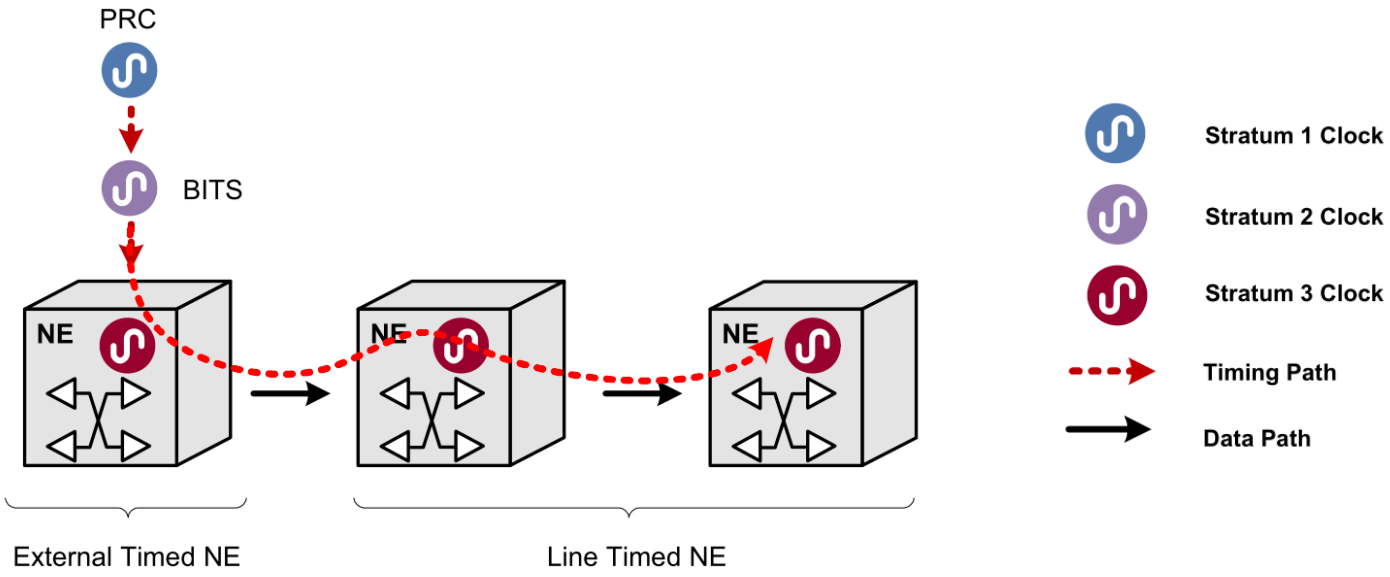
- External Timing: timing is input from external timing source, it is the most reliable method but expensive.

External Timing
Clock Distribution



External Timing and Line Timing

- Line Timing: the recovered clock at the receiving NE used as a timing source.

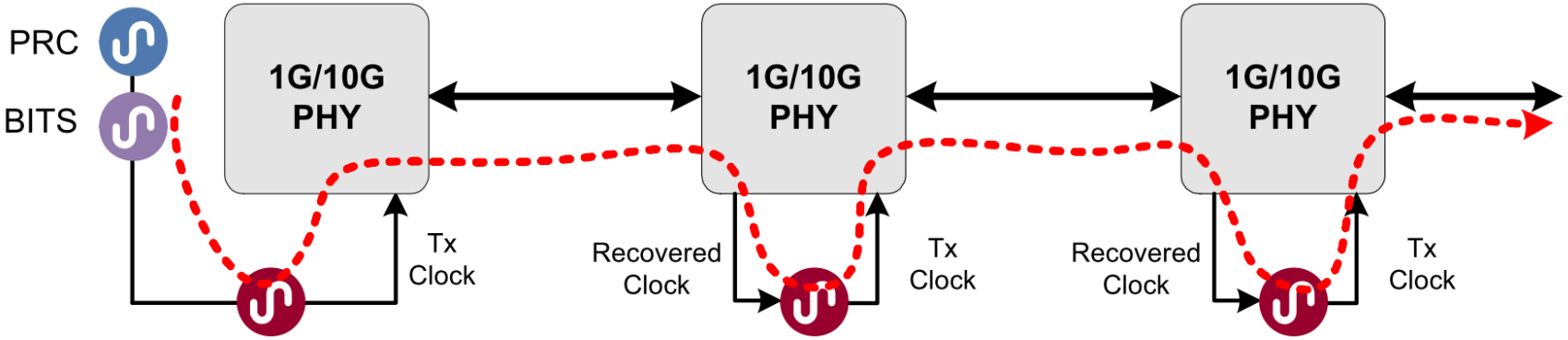


Synchronous Ethernet (SynE)

- Ethernet based packet networks are said to be asynchronous in nature. SyncE is a solution for Ethernet links to tranfer frequency .
- SyncE frequency synchronization is achieved through the physical layer in the same way that SONET/SDH line timing distributes its timing.

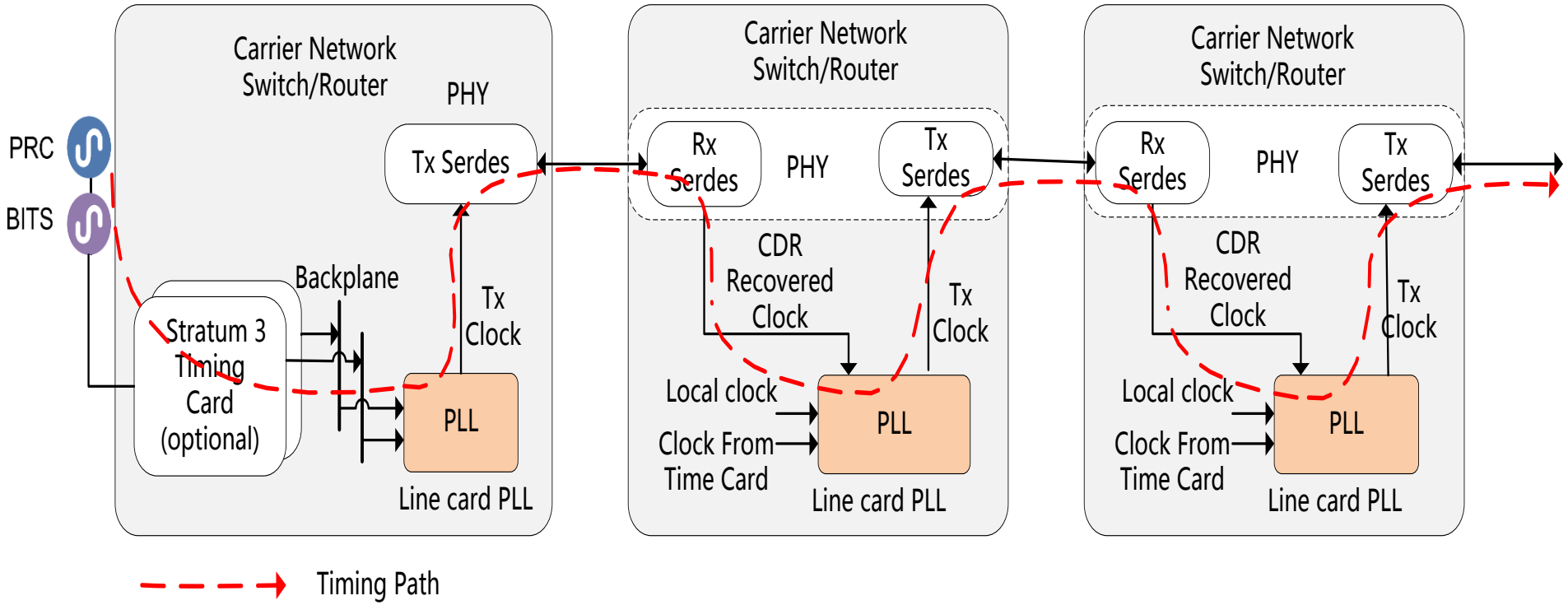
SyncE Physical Layer Frequency Synchronization

- A synchronization chain is formed by using a precise source at one end which is then recovered at downstream PHYs and retransmitted down the chain.



Why Frequency Synchronization need to be applied in FPGA?

How to implement Frequency Synchronization?

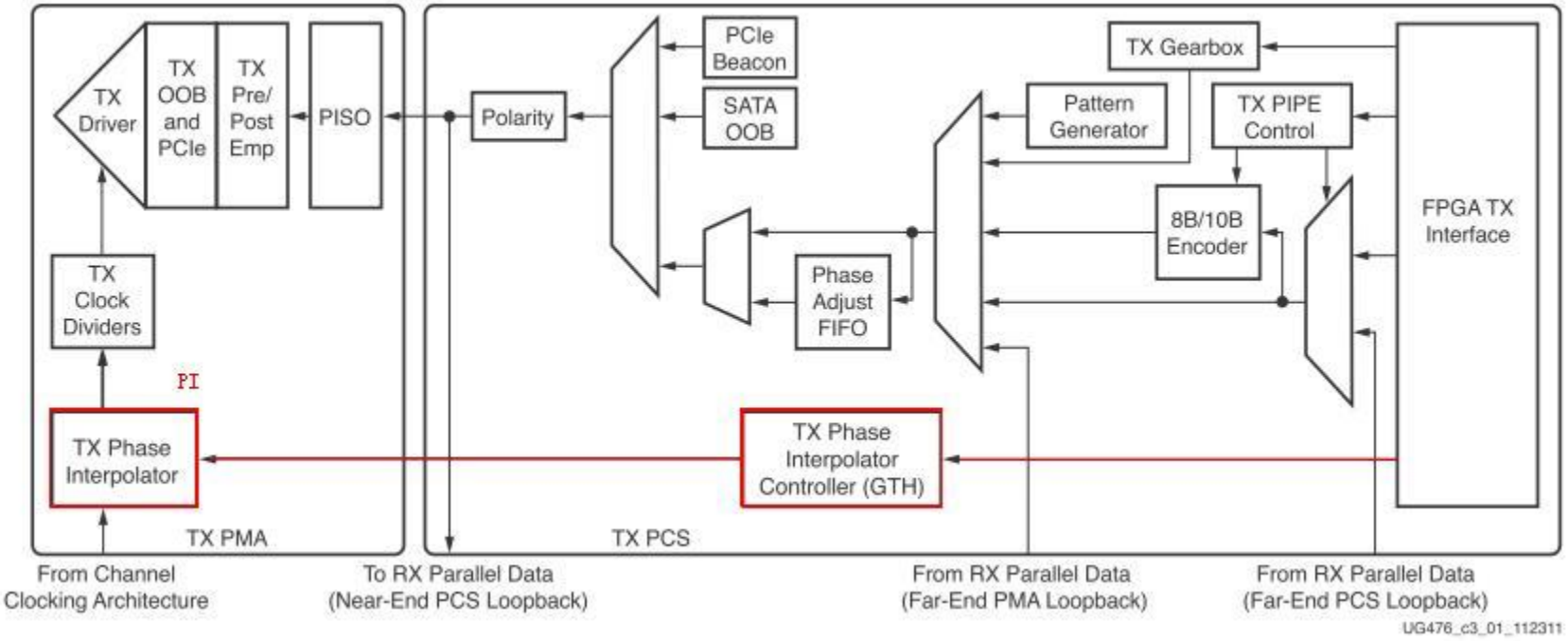


The disadvantage of using external PLL when many channels are in one card

- Significant BOM cost : every external PLL cost $10 to $15.
- Power consumption (300 mW to 500 mW) per additional PLL .
- Board space and PCB complexity, both due to additional board area required and careful noise-reduction design layout requirements.

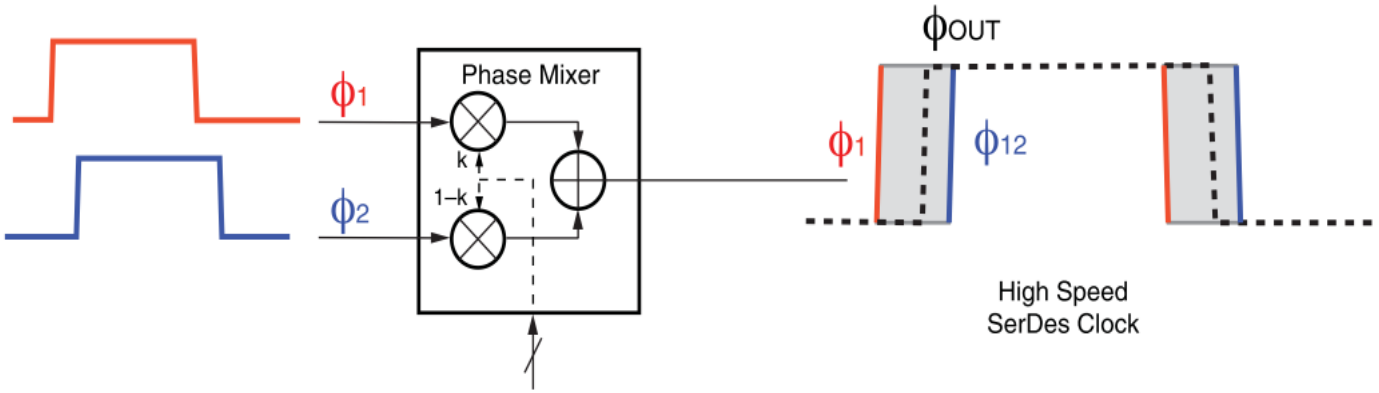
Contents

Phase interpolator(PI)



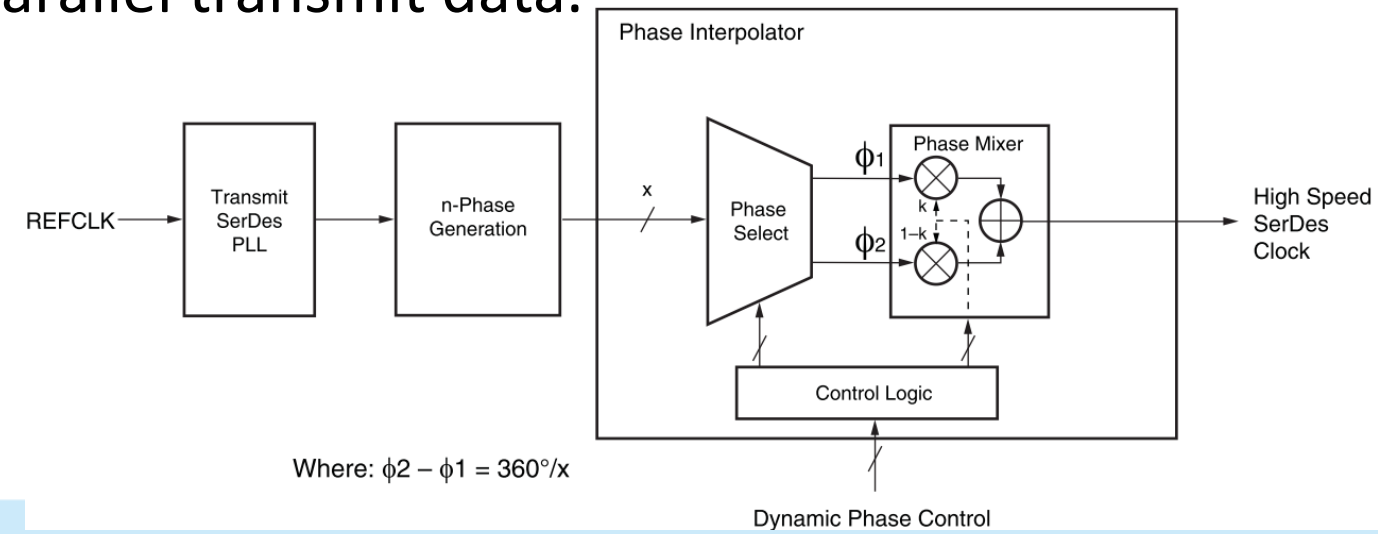
The Theory of Phase interpolator(PI)

- The phase interpolator function is performed by the phase mixer.
- Phase mixer combines different phase Φ1 and phase Φ2.The output is a clock with a phase that is in between phase Φ1 and phase Φ2.
- The phase interpolator produces a very low jitter clock with very fine phase resolution.



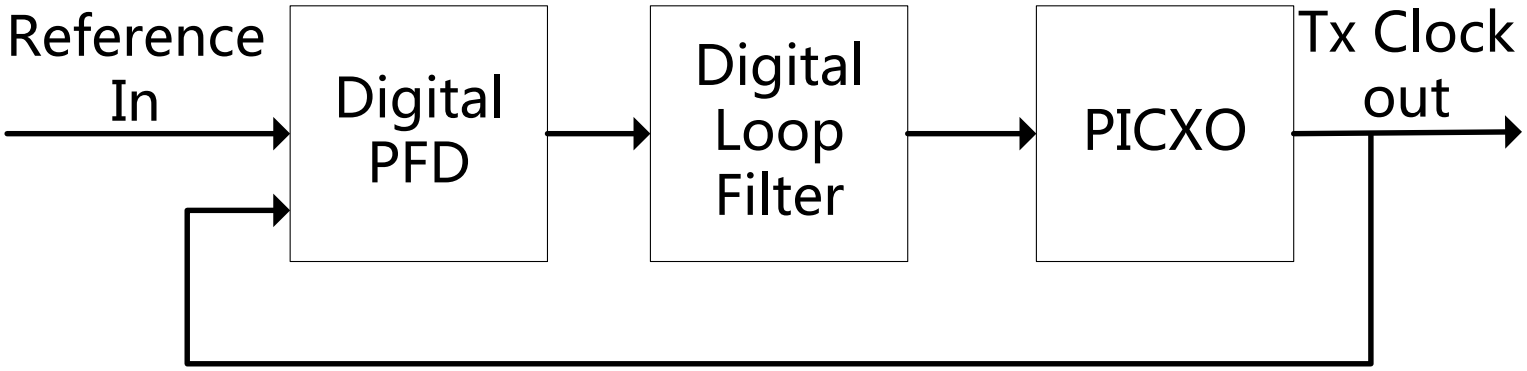
Transmit SerDes PLL work with PI

- SerDes transmit PLL produces a number of primary phases from the n-phase generation block.
- Phase select block selects two adjacent phases based on the control logic.
- A high-speed clock can be any one of 128 phases of the high-speed transmit clock used for serialization of the parallel transmit data.

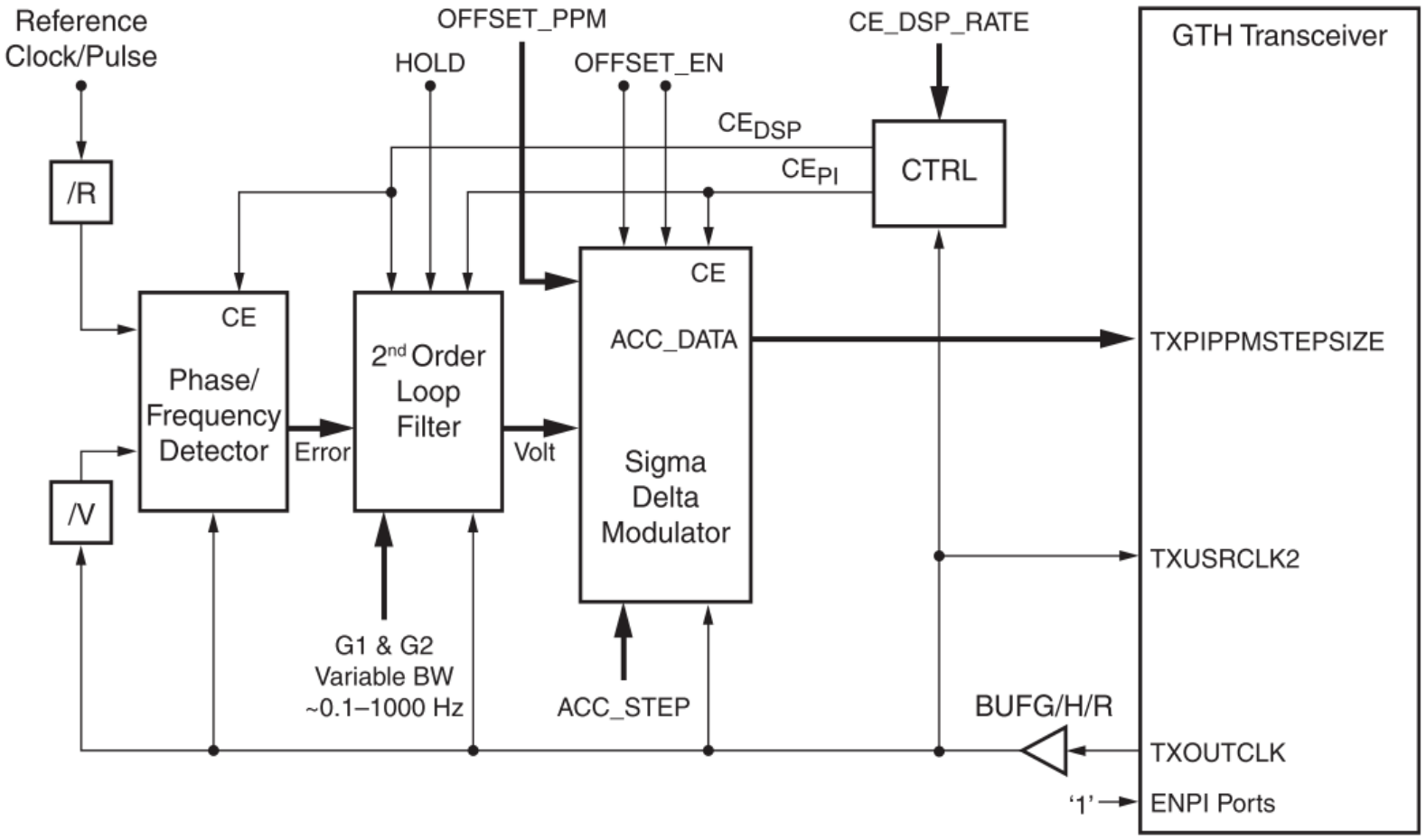


PICXO DPLL

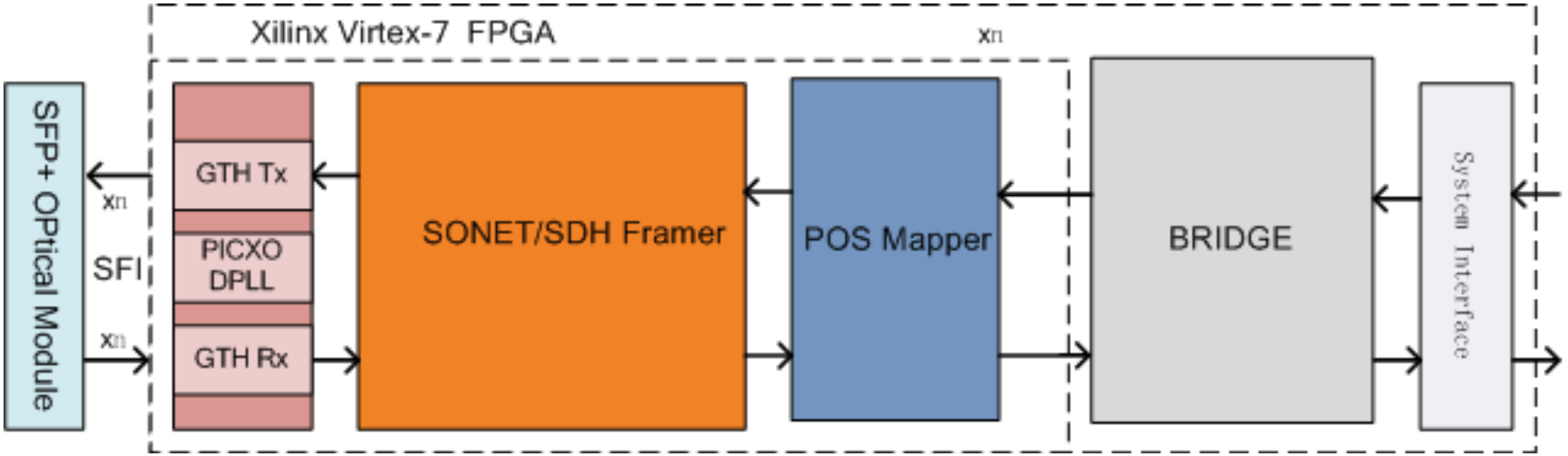
- The phase interpolator controlled crystal or Xtal oscillator (PICXO) DPLL is based on basic analog PLL.
- Digital Phase frequency detector(PFD)
- Digital Loop filter
- PICXO



PICXO DPLL Functional Block Diagram for GTH



Line Card with PICXO DPLL



Implement of frequency synchronization

- All ports of line card provide the ability of frequency synchronization,but use only one external PLL.
- Each transceiver provide a fully digital PLL (DPLL) by utilizing transceiver phase interpolator(PI). The transmitter can phase or frequency lock to receiver.
- If GTH Rx CDR lost to lock input datastream, PICXO DPLL will enter holdover mode,and output previous frequency which acquired during normal mode.

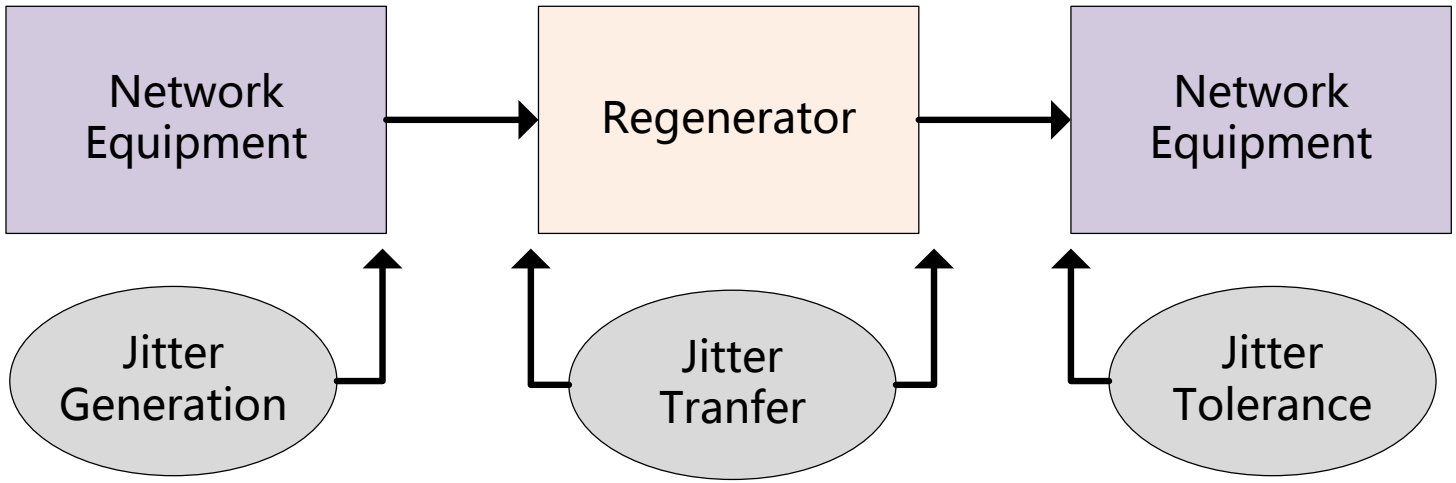
Contents

Introduction to Jitter

- Jitter and wander are two of the most important considerations in a synchronization system.
- Jitter is defined as any phase modulation above 10 Hz in a digital signal,and wander is noise below 10 Hz.
- It is important that there are limits for the maximum level of jitter at an output interface and for the maximum level that can be tolerated at an input.
- The following section will show the jitter test result of 10G POS line card.
- SONET Jitter specifications :Telcordia GR-253

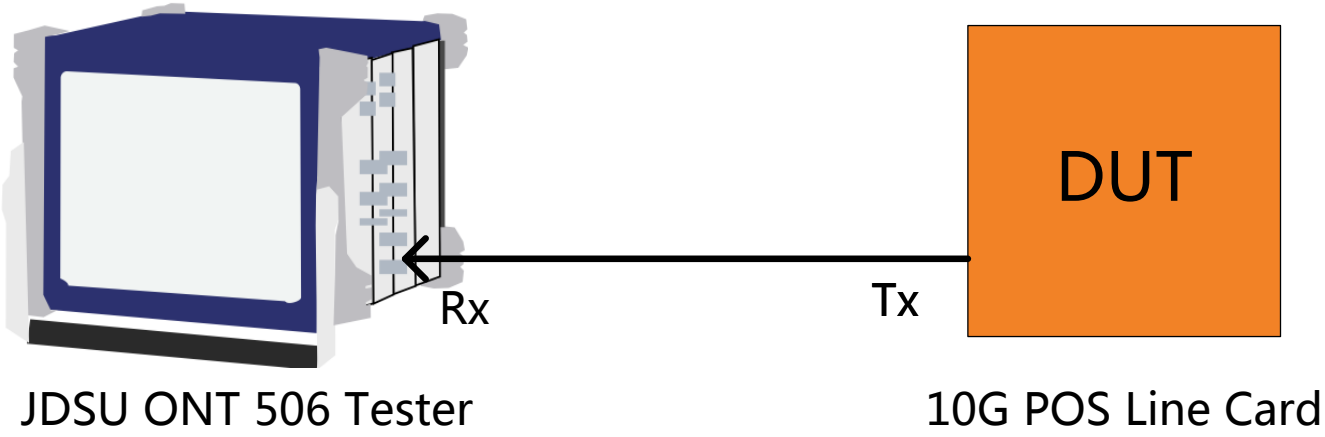
Jitter performance of a transmission system

- There are three relevant measurements that define the jitter performance of a transmission system:
- Jitter Generation
- Maximum Tolerable Jitter(MTJ)
- Jitter Transfer Function(JTF)



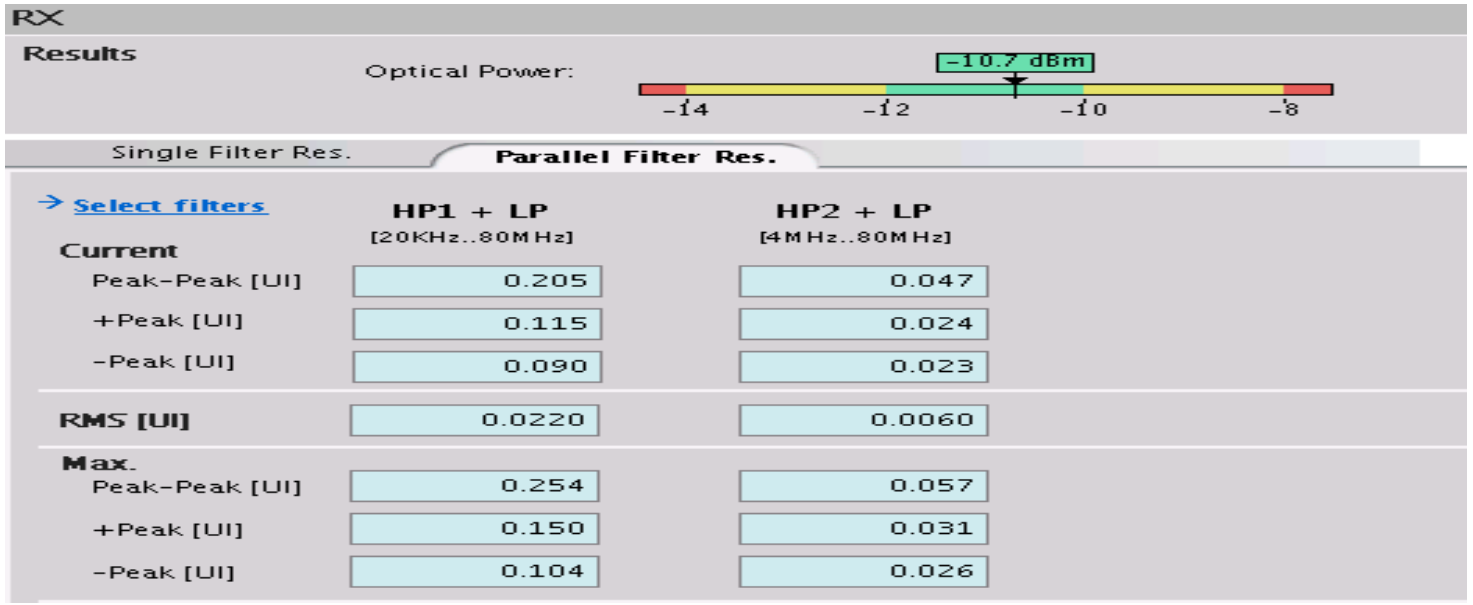
Jitter Generation(Output jitter)

- Output jitter is the overall jitter measured at the output of a system.
- Here is output jitter measurement environment.



Output Jitter Requirements and Results

Interface	Measuring filter	Peak-to-peak amplitude	Test Results
OC-192/ STM-64	20 kHz to 80 MHz	0.30 UI	0.254 UI
	4 MHz to 80 MHz	0.10 UI	0.057 UI


RX

Results

Optical Power: -10.7 dBm

-14 -12 -10 -8

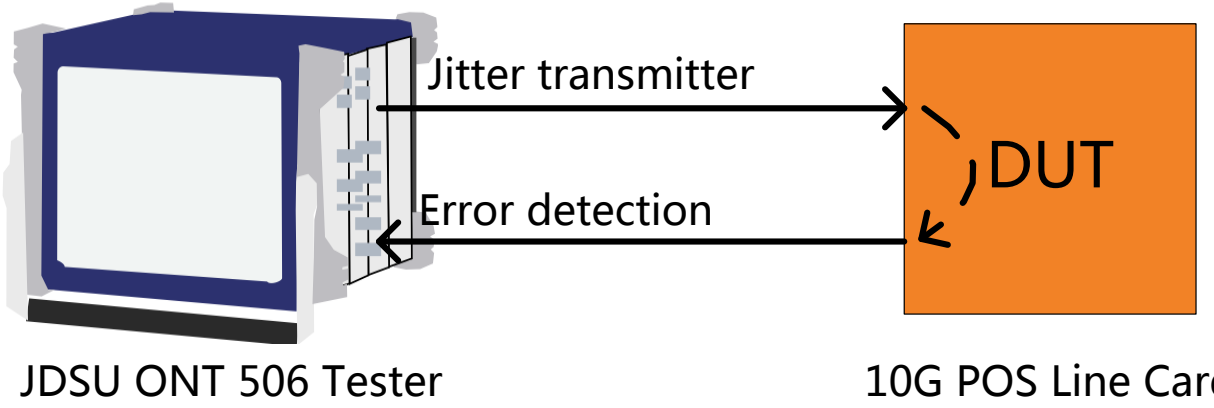
Single Filter Res. | Parallel Filter Res.

Select filters

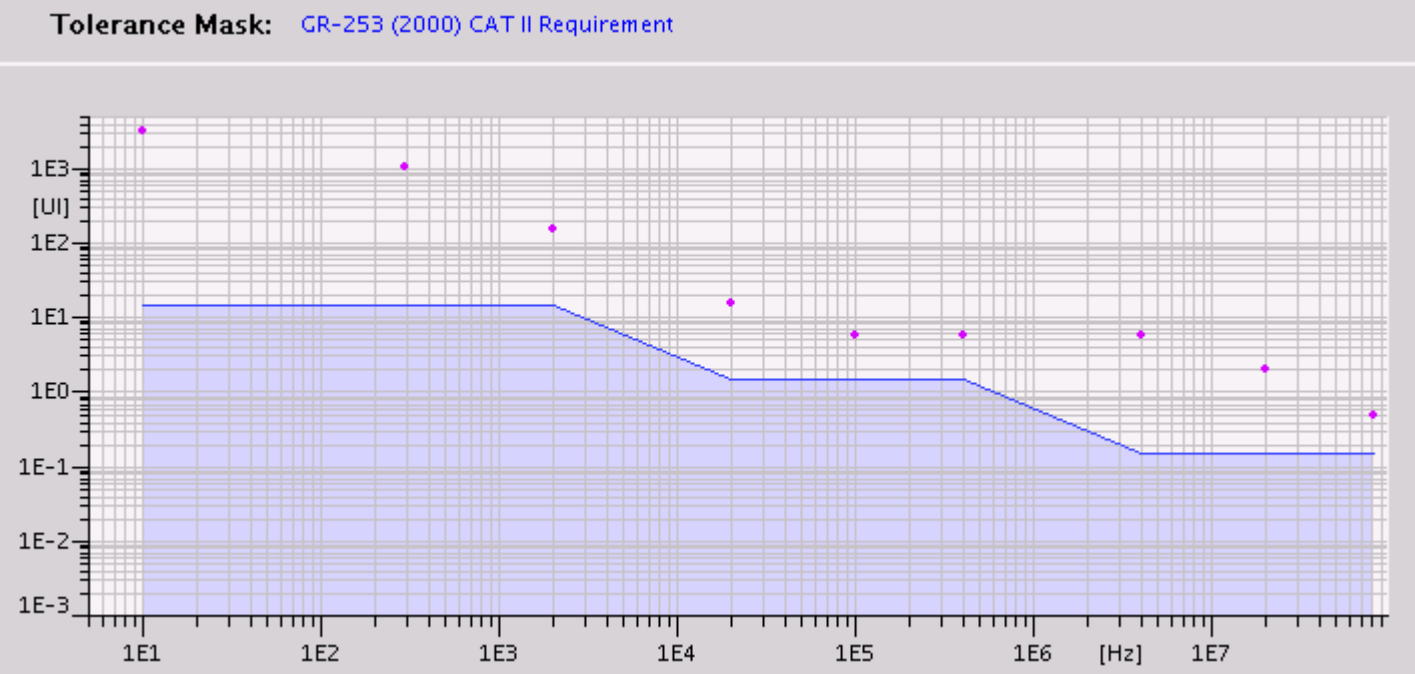
	HP1 + LP [20KHz..80MHz]	HP2 + LP [4MHz..80MHz]
Current		
Peak-Peak [UI]	0.205	0.047
+Peak [UI]	0.115	0.024
-Peak [UI]	0.090	0.023
RMS [UI]	0.0220	0.0060
Max.		
Peak-Peak [UI]	0.254	0.057
+Peak [UI]	0.150	0.031
-Peak [UI]	0.104	0.026

Maximum Tolerable Jitter(MTJ)

- Jitter tolerance is a measurement to check the resilience of equipment to input jitter.
- Jitter tolerance is one of the most important characteristics of the clock recovery and input circuitry of network equipment.

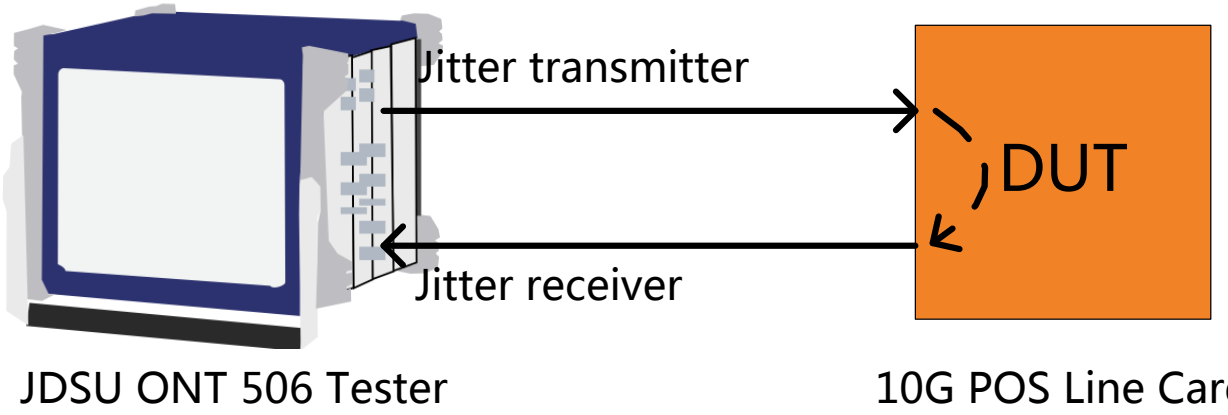


MTJ Graphic Results

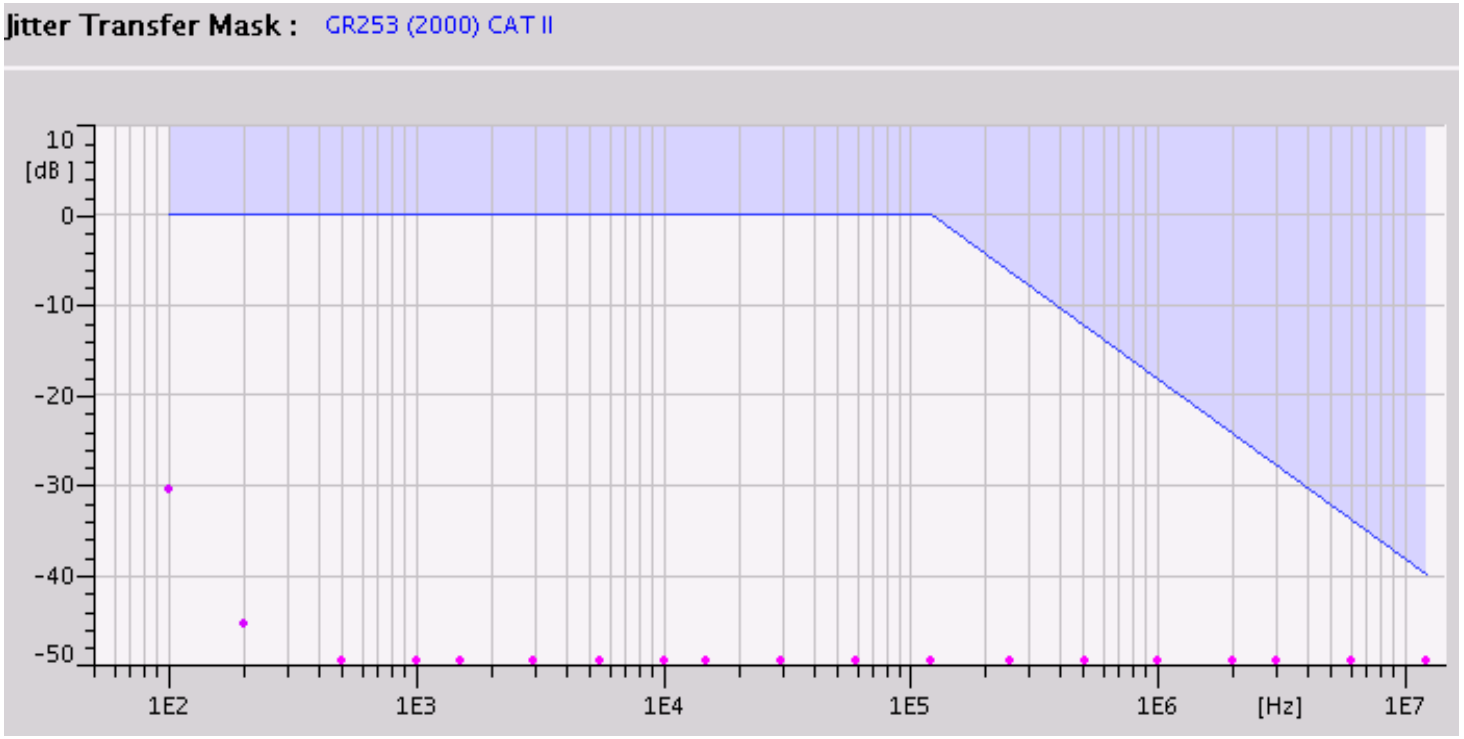


Jitter Transfer Function(JTF)

- Jitter transfer is a measure of how much jitter is transferred from the input to the output of the network equipment.
- JTF is important for cascaded clock recovery circuits in long-distance transmission systems with regenerators and line terminals.



Jitter Transfer Function Graphic Results



Results of Jittter Test

- Results of Jitter test show that Xilinx Virtex-7 device and PICXO DPLL can be compatible with SONET/SDH specification.

Contents

Summary

- Carrier networks have a strong requirement of frequency synchronization across the network.
- There are some disadvantages of using external timing mode or line timing mode with external PLL: high cost, additional power consumption and complex design.
- How to implement frequency synchronization in FPGA.
- The results of Jitter test show that Xilinx Virtex-7 device and PICXO DPLL can be compatible with SONET/SDH specification.

Bringing you Closer

Thanks!